WHAT IS CLAIMED IS:

1. A frequency shift keyed (FSK) receiver capable of demodulating an incoming transmitted signal comprising:

a phase-locked loop for receiving an oscillator reference signal having a frequency F1 and generating a reference carrier frequency signal having a desired frequency N1(F1), wherein N1 may be a non-integer value, said phase-locked loop comprising:

a phase detector having a first input for receiving said oscillator reference signal and a second input; and

a frequency divider circuit for dividing an actual frequency of said reference carrier frequency signal by an adjustable integer value N2 applied to a control input of said frequency divider circuit to thereby generate a feedback signal applied to said second input of said phase detector;

a frequency discriminator that receives said incoming transmitted signal and said reference carrier frequency signal and generates a correction signal corresponding to a difference between a center frequency of said incoming transmitted signal and said actual frequency of said reference carrier frequency signal; and

a delta-sigma modulator controlled by said correction signal operable to generate a sequence of integers having an average value of N1 over a defined time period, wherein said sequence of integers are applied to said control input of said frequency divider circuit.

2. The FSK receiver as set forth in Claim 1 further comprising a subtraction circuit capable of subtracting said correction signal from a nominal carrier frequency value to thereby generate a control frequency signal that controls said delta-sigma modulator.

3. The FSK receiver as set forth in Claim 1 wherein frequency discriminator comprises a first mixer that receives said incoming transmitted signal and said reference carrier frequency signal and generates an intermediate frequency signal having a frequency equal to a difference between said center frequency of said incoming transmitted signal and said actual frequency of said reference carrier frequency signal.

4. The FSK receiver as set forth in Claim 3 wherein frequency discriminator further comprises a signal splitter that splits said intermediate frequency signal into a first child intermediate frequency signal and a second child intermediate frequency signal.

5. The FSK receiver as set forth in Claim 4 wherein frequency discriminator further comprises a delay element that delays said second child intermediate frequency signal by a delay, T.

6. The FSK receiver as set forth in Claim 5 wherein said delay, T, is a substantially equal to a quarter wavelength of said second child intermediate frequency signal.

7. The FSK receiver as set forth in Claim 5 wherein frequency discriminator further comprises a second mixer that receives said first child intermediate frequency signal and said time-delayed second child intermediate frequency signal and generates a DC correction voltage.

8. The FSK receiver as set forth in Claim 7 wherein said frequency discriminator further comprises an analog-to-digital converter that receives said DC correction voltage and outputs said correction signal.

9. A method of demodulating a transmitted signal comprising the steps of:

mixing the transmitted signal and a reference carrier frequency signal having a desired frequency N1(F1), wherein N1 may be a non-integer value, produced by a phase-locked loop (PLL) to generate a correction signal corresponding to a difference between a center frequency of the transmitted signal and an actual frequency of the reference carrier frequency signal;

in the phase-locked loop (PLL), dividing the actual frequency of the reference carrier frequency signal by an adjustable integer value N2 applied to a control input of a frequency divider circuit to generate a PLL feedback signal having a frequency of (N1/N2)F1;

in the phase-locked loop, comparing the phase of an oscillator reference signal having a frequency F1 and the phase of the PLL feedback signal and using the phase difference to control a voltage controlled oscillator generating the reference carrier frequency signal having the desired frequency N1(F1); and

using a delta-sigma modulator controlled by the correction signal to generate a sequence of integers having an average value of N1 over a defined time period, wherein the sequence of integers are applied to the control input of the frequency divider circuit.

10. The method as set forth in Claim 9 further comprising the step of subtracting the correction signal from a nominal carrier frequency value to thereby generate a control frequency signal that controls the delta-sigma modulator.